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CPE 409 Lab 2

# Goals

1. Learn how to ensure that the main loop never fully completed by using an infinite “while” loop
2. Learn how to manipulate logic statements and “while” loops to create a simple delay.
3. Learn how to interface the timer peripheral for the dsPIC33
4. Learn how to use the stopwatch and the logic analyzer in MPLAB SIM

# Equipment used

## Hardware

* Microchip Explorer 16 board
* PIC kit 3

## Software

* MPLAB X IDE 2.00

# Design Specifications

* Must never exit the “main” function
* Must use the lower bits of PORTA to perform the following tasks:
  1. Turn PORTA on for .5 second
  2. Turn PORTA off for 0.5 second
  3. Repeat

# Design

* Refer to Figure 1 for the flow diagram of the design

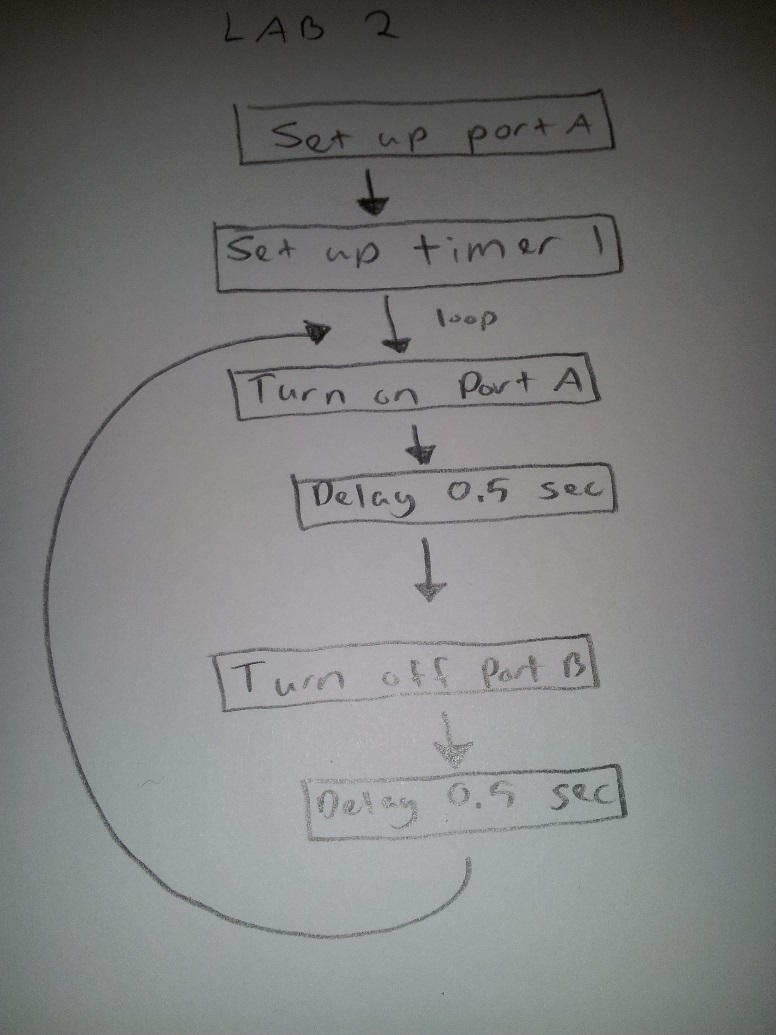


Figure 1: Flow diagram of the design

* See the end of the report for the code for the program

# Verification

MPLAB X Simulator was used to verify the program. Verification of the program was divided into two parts.

* Part 1: Timing verification
  1. The timing of the program was verified using the stopwatch function of MPLAB X.
  2. Break points were set before each of the delays used in the program, and the output of the stopwatch was recorded.
     1. See figure 2 for the output of the stopwatch.

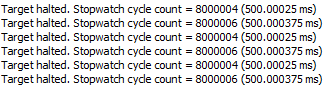


Figure 2: Output of MPLAB X stopwatch

* Part 2: Logic verification
  1. The output logic of the program was verified using MPLAB X logic analyzer function
  2. The program was allowed to run and the output of RA7 was observed using the logic analyzer to ensure that the bit is being toggle properly.
     1. See figure 3 for the output of the logic analyzer.

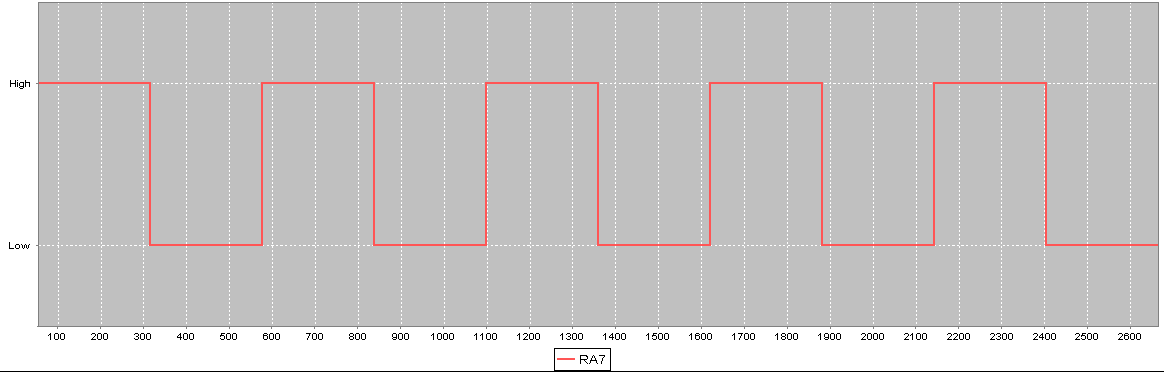


Figure 3: Output of MPLAB X logic analyzer

# Questions

1. What is this period measured and why is it not take exactly 256 instructions?

16 us. It does not take exactly 256 instructions because a jump instruction in assembly takes more than 1 instruction cycle.

# Conclusions and Limitations

It was concluded that the design meet all the specification requirements. The limitation that was discovered through this lab was the limitation with MPLAB X logic analyzer function. Although the logic analyzer function allows one to observe the logic of the program, it does not allows one to properly see the timing of the system.